12.8 A 13b Linear 40MS/s Pipelined ADC with Self-Configured Capacitor Matching

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Current CMOS processes offer MIM capacitors that match to about 0.1%, often limiting the achievable accuracy of Nyquist-rate pipelined ADCs to 10 to 12 bits. To achieve higher resolutions, it is required to correct lithographic errors. Digital calibration techniques have been successfully demonstrated for MDAC based pipelined ADCs [1, 2, 3, 4]. However, analog calibration has the unique advantage of applying corrections right at the source of the error rather than compensating for them later digitally [5, 6]. Analog calibration techniques usually use resistor or capacitor trimming network, and it is cumbersome to extend the same concept to correct the errors in multi-bit MDACs. In this work, an alternative solution equivalent to analog trimming is proposed, in which the errors in the capacitors are used as the corrective elements themselves. An algorithm is proposed to correct the mismatch errors in a multi-bit MDAC by breaking each unit DAC capacitor into smaller elements and reconstructing them by grouping in a way that the errors get cancelled. This statistical matching scheme can be used to correct for the errors in an array of many nominally identical elements such as the DAC in a ΔΣ ADC or current-steering DACs.

Combining n identical elements with standard deviation σ will cause the effective standard deviation to decrease by the square root of n. However, knowledge of the individual values allows elements to be combined such that the grouped elements can be better matched. This can be explained by a simple example, shown in Fig. 12.8.1, where two nominally identical elements are made with two half ones each. The elements from this pool of four can be recombined into two groups in three different ways, out of which one has a smaller spread than the other ones. A configuration can be found in which a positive error is used to cancel a negative error such that the effective combined capacitors have the least possible spread. This principle is extended to a pool of 32 sub-elements from which four groups have to be made by permuting the elements in various ways and measuring the spread. It is not practical to examine all of the nearly 2.5×10^{16} possible configurations. The proposed algorithm explores the solution space in a random walk fashion. Simulations show rapid convergence to a 14b 3σ matching from a 10b σ-matched array after about 500 to 1000 random tries. This capacitor-matching algorithm is used in a 3b tri-level MDAC using 4 capacitors. Note that 32 elements and 16 elements of 62.5fF each are used to form the 2pF sampling capacitor used in the first stage and the 1pF sampling capacitors used in the second and third stages. The ADC system based on this is shown in Fig. 12.8.2.

The choice of the best-matched configuration among many tried ones relies on accurate MDAC error measurement, which is basically the same measurement technique as used in standard ADC calibration techniques. Both foreground and background measurement techniques for DAC and opamp finite gain errors are well known. In this work, the algorithm is run offline (foreground), since capacitor errors do not change much over time and temperature. To calculate a measure of the spread, all the capacitors are measured as in [1] against each other using a sequence defined by the "state-sequencer" block, shown in Fig. 12.8.3. The spread is measured and updated along with the array configuration details in an on-chip memory whenever a lower spread is encountered. This self-configuration sequence is designed such that the stages that resolve the lesser significant bits are configured before the stages that resolve the more significant bits. A key component in the system is a permutation generator. It is necessary to be able to span the whole permutation space using logic that is also easy to implement. Existing techniques like using unit swaps become very complicated when permuting large number of elements. Simple butterfly shufflers and barrel shifters cover only a small subset of the possible permutation space. A state machine approach is taken where the state transitions are derived from elementary transformations of elements moved on the surface of a cube. Assume that the elements (1, 2, … , 24) that are permuted occupy positions on the surface of a cube. This forms a known valid configuration. Define 6 paths on the surface of the cube (eg., 1→2, 2→4, 4→3, 3→1) and 3 paths along the volume (eg., 1→2, 2→5, 5→6, etc.). One of these 9 paths is chosen by the output of a pseudo-random word generator along which the elements move to form a new permutation. These transition rules allow close to unique permutations to be generated. The 24-element case is easy to visualize, but 32 or 16 elements can be also efficiently permuted with a state repetition ratio (defined as the ratio of total states generated to the number of unique states) close to 1 with simple logic circuits.

The opamp is a two-stage Miller-compensated amplifier with a telescopic gain boosted first stage followed by a common-source output stage as shown in Fig. 12.8.4. Switches in the signal path are boosted. The timing critical path that combines the outputs of the sub-ADC and the permutation address vector to generate the switch control signals are designed using custom logic to minimize the path delay. The prototype IC is fabricated in a 0.18μm CMOS. It occupies $3.6mm^2$ and consumes 168/100mW (analog/digital) at 40MS/s from a 1.8V supply. The input range is $1.6V_{pp\text{-}diff}$. After configured for low spread, capacitor matching is visibly improved in the INL measurement from 3LSB to 0.8LSB as shown in Fig. 12.8.5 and the measured DNL is 0.4LSB. With 14MHz input sampled at 43MS/s, measured SFDR is also improved from around 70dB to >80dB after configured as shown in Fig. 12.8.6. Measured THD and SNDR are -73dB and 67dB. The capacitor-array MDACs in the first, second, and third stages exhibit linearity of 5, 2, and 1LSBs at 16b level, respectively, after 5018, 1285, and 5122 random trials. It takes about 2 seconds to configure three MDAC stages for low spread. The die micrograph is shown in Fig. 12.8.7.

Acknowledgements:
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References:
[1] S. Lee and B. Song, "Digital-Domain Calibration Techniques for Multistep Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1679-1688, Dec., 1992.
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[6] S. T. Ryu, et al., "A 14-b Linear Capacitor Self-Trimming Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2046-2051, Nov., 2004.

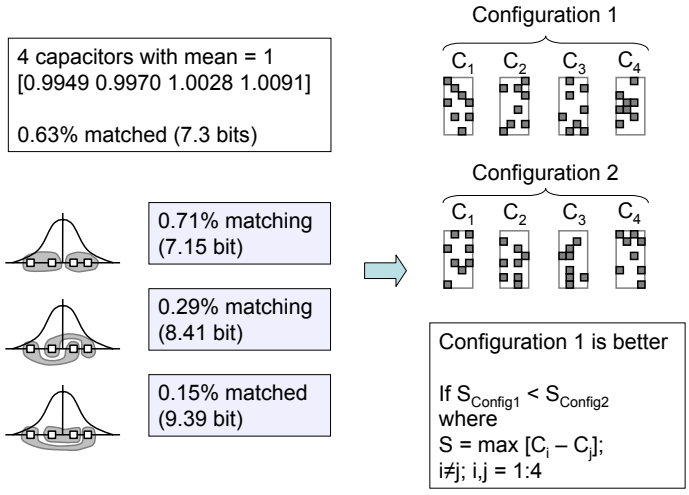

Figure 12.8.1: Example showing improvement in matching using different combinations, and extension of the principle to larger arrays.

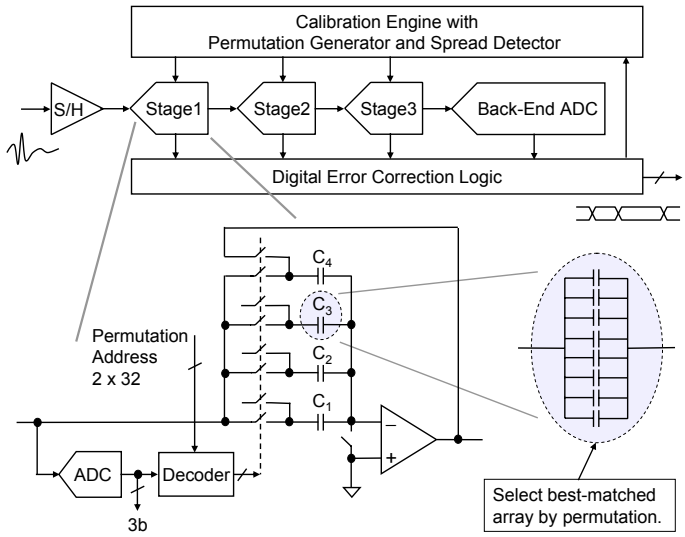

Figure 12.8.2: Pipelined ADC with capacitor array configured for best matching.

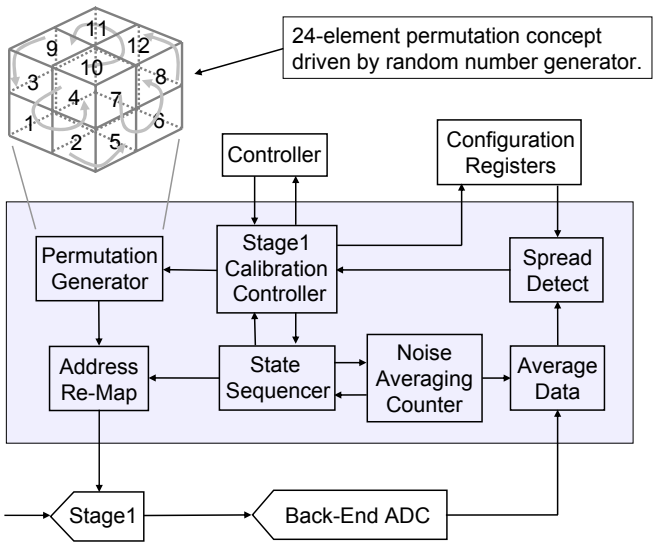

Figure 12.8.3: Calibration algorithm per stage, 32/16 elements are permuted.

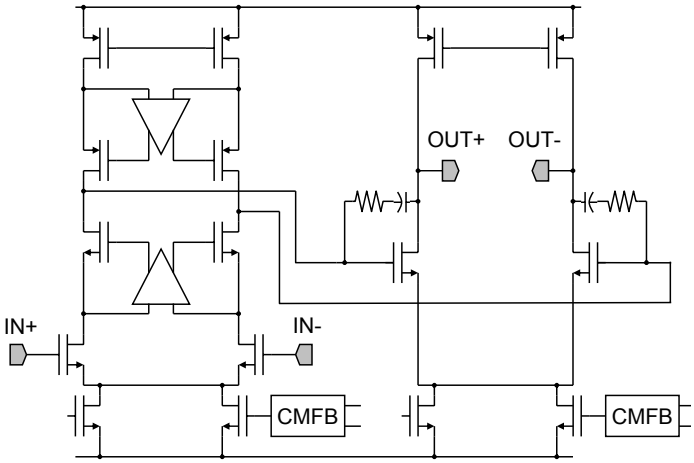

Figure 12.8.4: Opamp schematic.

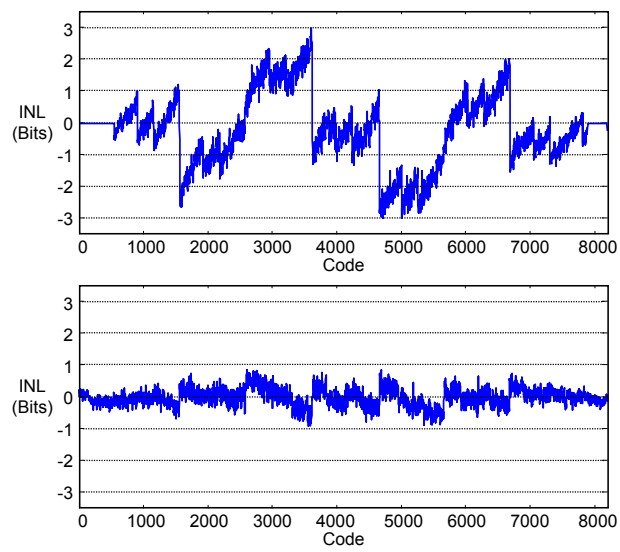

Figure 12.8.5: Measured INL @13b level before and after configuring for low spread.

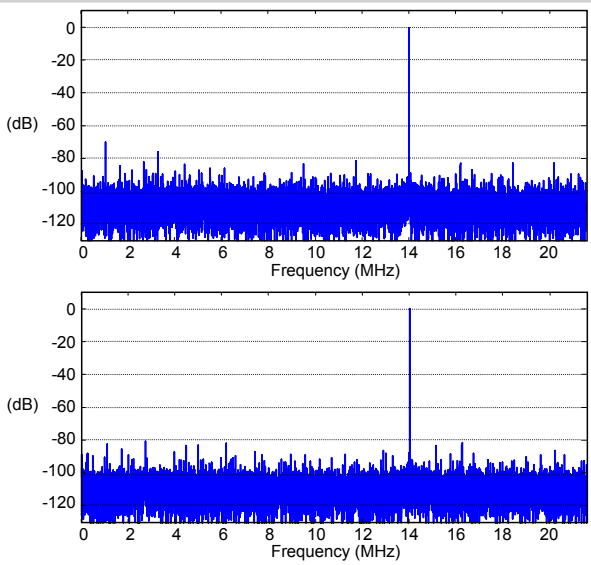

Figure 12.8.6: 14MHz sampled at 43MS/s before and after configuring for low spread.

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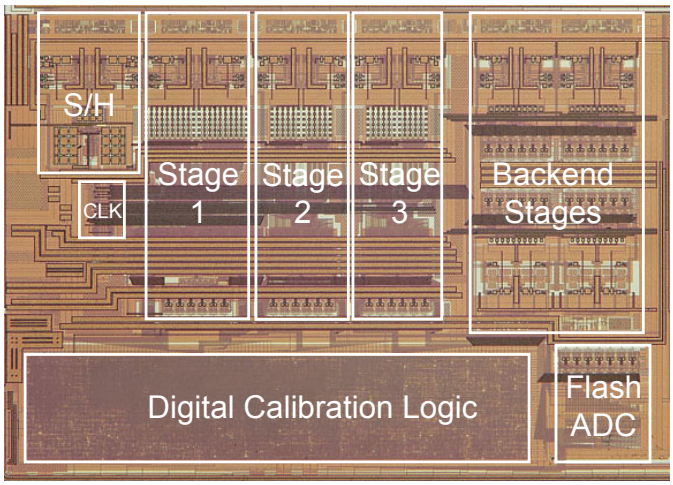

Figure 12.8.7: Chip micrograph.

